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U.S. PATENT DOCUMENTS

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Yasuhiko Nakashima, et al., "Multilevel Reuse and Parallel Precomputation Based on Dynamic Instruction Analysis", Article of Journal of Information Processing Society, Computing System, Information Processing Society, July 2003, Vol. 44, No. SIG 10 (ACS 2) (20030715), pp. 1-16 (together with its partial English translation)

Notice of Allowance for Japanese Patent Appln. No. 2004-097197 mailed January 20, 2009 with English translation

***Examiner**

/Idriss Alrobaye/

Date Considered

02/09/2010

Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Initial a this form with next communication to applicant.